Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.120”**

**4 3 2 2 1 28 27 26**

**25**

**24**

**23**

**22**

**21**

**20**

**19**

**18**

**4**

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**11**

 **12 13 14 15 16 17**

**PAD FUNCTIONS:**

1. **V IN**
2. **AGND1**
3. **REF**
4. **CAP**
5. **AGND2**
6. **D15 (MBS)**
7. **D14**
8. **D13**
9. **D12**
10. **D11**
11. **D10**
12. **D9**
13. **D8**
14. **DGND**
15. **D7**
16. **D6**
17. **D5**
18. **D4**
19. **D3**
20. **D2**
21. **D1**
22. **D0 (LSB)**
23. **BYTE**
24. **R/C**
25. **CS**
26. **BUSY**
27. **V ANA**
28. **V DIG**

**.220”**

**Top Material: Al**

 **Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .120” X .220” DATE: 8/18/16**

**MFG: ANALOG DEVICES THICKNESS .020” P/N: AD976**

**DG 10.1.2**

#### Rev B, 7/1